(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/17580 A1

(51) International Patent Classification[7]: H04L 12/64

(21) International Application Number: PCT/US01/26567

(22) International Filing Date: 23 August 2001 (23.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/228,008 23 August 2000 (23.08.2000) US
60/272,793 1 March 2001 (01.03.2001) US

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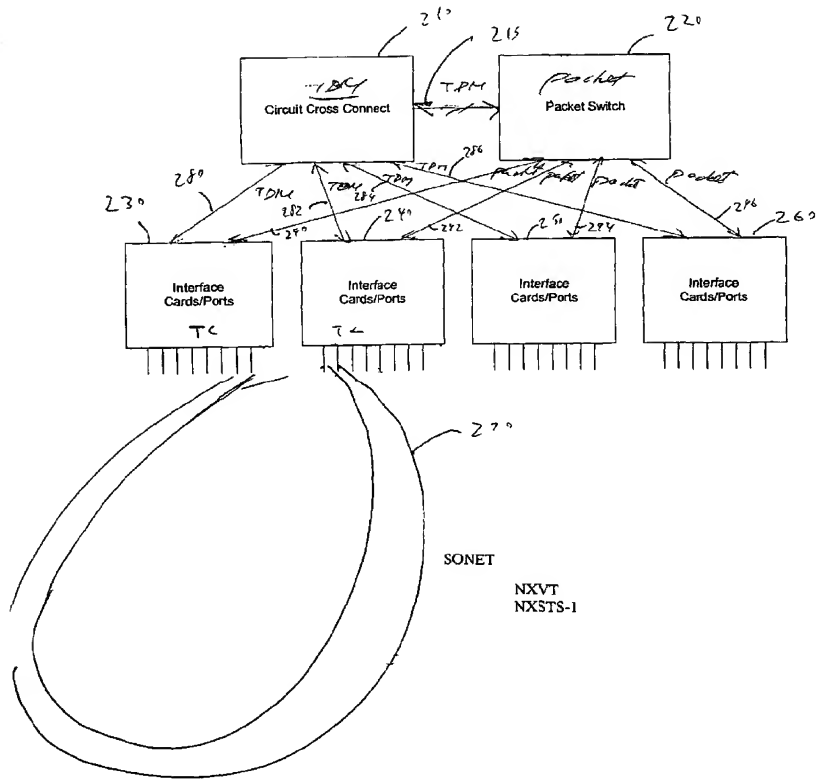
(81) Designated States *(national)*: AU, BR, CN, DE, DK, ES, GB, IN, JP, KR, MX, PT, SG.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DUAL SWITCH ARCHITECTURE FOR MIXED PACKET AND CIRCUIT TRANSPORTS OVER SONET AND SDH AND DWDM



(57) Abstract: A dual switch architecture (200) for mixed packet and circuit transports over SONET and SDH and DWDM is provided. The dual switch architecture includes a TDM circuit cross connect module (210), a packet switch module (220), interface modules (230) with one or more ports, a bi-directional TDM bus (215) between the TDM circuit cross connect module and the packet switch module, a point-to point, bi-directional TDM connection (280) between each interface module and the TDM circuit switch module, and a point-to point, bi-directional packet connection (290) between each interface module and the packet switch module.

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DUAL SWITCH ARCHITECTURE FOR MIXED PACKET AND CIRCUIT TRANSPORTS OVER SONET AND SDH AND DWDM

SPECIFICATION

RELATED APPLICATIONS

This application is related to U.S. Provisional Application No. 60/228,008, filed on August 23, 2000, to U.S. Provisional Application No. 60/272,793 , filed on March 1, 2001, to co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-014, filed on August 23, 2001, and to co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-015, filed on August 23, 2001. The contents of U.S. Provisional Application No. 60/228,008, filed on August 23, 2000, of U.S. Provisional Application No. 60/272,793, filed on March 1, 2001, of co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-014, filed on August 23, 2001, and of co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-015, filed on August 23, 2001, are hereby incorporated by reference. This application claims priority to U.S. Provisional Application No. 60/228,008, filed on August 23, 2000, and to U.S. Provisional Application No. 60/272,793, filed on March 1, 2001.

FIELD OF THE INVENTION

The present invention relates to optical networking. More particularly, the invention relates to a dual switch architecture for mixed packet and circuit transports over SONET and SDH and DWDM.

BACKGROUND OF THE INVENTION

Both SONET (See Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria. GR-253-CORE, Issue 2, Revision 1. December, 1997.) and SDH (See International Telecommunication Union. Network Node Interface for the Synchronous Digital Hierarchy. Recommendation G.707. March, 1996.) enable the use of virtual concatenation to support both the dynamic resizing of transport trunks and the grooming of traffic. More recently, advances in the transport of routed datagram traffic leveraging the research and experience of ATM has resulted in the standardization of MPLS (See Internet Engineering Task Force. Multiprotocol Label Switching Architecture. IETF Draft Document. August, 1999 and http://www.ietf.org/internet-drafts/draft-ietf-mpls-arch-06.txt.). This work allows network devices to employ a standards-based method by which packet traffic can traverse a network, while receiving a previously agreed upon Quality of Service.

Pure Circuit/Packet Connection Switch

Existing architectures usually handles either circuit connection or data connections separately. In either circuit or packet connections, two major multiplexing/switching structure exist. One is the hub structure, which allows many connections to share a common bus/bandwidth. The other is the switch/cross connect structure, which allows the share of each destination port/bandwidth independently. The main difference between the hub structure and the switch structure is on the performance. The hub structure limits all ports to share a common bandwidth, while the switch structure allows all ports to share each individual output port bandwidth. In this way, the total aggregated bandwidth of the switch can be many times higher than the hub structure.

Hub Structure

Referring to Figure 1A, a prior art hub structure with a typical add/drop multiplexer uses a shared tri-state bus structure to multiplex/de-multiplex the interface port traffic to/from the common media. In circuit connection, all ports are attached to the shared back-plane bus directly through a tri-state buffer. A pre-configured time slot is

assigned to each port according to the provisioning need. To add traffic to the ring, each port simply turns on the tri-state buffer to drive the bus at a correct time slot. To drop traffic from the ring, every port monitor the drop bus all the time and catch traffic at the correct time slot. In this way, one global time-slot is used on the hub bus is used. All ports basically follow the time slot assignment.

In packet connection, hub structure uses a media access control layer to determine which packet (of certain port) gets the right to access the common media. The decision is on a per packet base. A typical example for hub structure is the Ethernet. It uses carrier sense multiple assess/collision detection to arbitrate the use of the shared common cable, and evenly assign the access right to every port. The hub structure can use either a bus structure (e.g., coaxial cable in Ethernet), or a star-shaped hub (e.g., Ethernet repeater hub). In the star-shaped hub, the internal arbitration mechanism still follows the same media access control protocol.

Switch Structure

Referring to Figure 1B, a prior art switch structure with a typical cross switch engine for circuit connections uses a cross-connect switching fabric at a centralized location. Every interface ports talks to the centralized cross connect engine directly in a star fashion. A pre-configured source to destination port map is used for the engine to determine how to switch the traffic. A pre-assigned time-slot table is used in each of the output port. I.e., it would be N tables if there are N output ports. Through the cross connect engine, a circuit in one port can be mapped to a circuit of any other port. Further more, circuits in different ports can be mapped/aggregate into the same output port. This achieves the switching of unicast/multicast connections from any input ports to any destination, performing grooming, etc. The total switching bandwidth can be N times the bandwidth of a hub.

The switching engine for packet connection is similar to circuit connection, except that the decision of accessing right on each output port is determined on a per packet based. It uses the packet header information to dynamically determine the switching destination port. Then it uses certain arbitration mechanism, such as weighted round-robin or priority round-robin to assign the right to access each output port.

Mixed Packet/Circuit Switching

To support mixed packet/circuit switching, there are several possible solutions.

Circuit Based Switching

Referring to Figure 1C, a prior art circuit based switching design of mixing both packet and circuit switching is to use circuit switching as a basic platform. The packet connections are first processed and put into a pre-configured connection. Then it uses a circuit switching fabric to do the switching for both circuit and packet. The packet support is basically a front end processing in a circuit connection. A common example is to use the traditional telephone voice connections to support packet data through the MODEM as a front-end processor. In this way, all switching rely on the circuit switching. This solution is a limited solution and lack of the flexibility to do packet processing locally.

The disadvantage of the circuit based switching for packet switching is the lack of flexibility in both configuration and bandwidth utilization efficiency. The circuit based switching used for packet switching requires the packet connection to use a fixed configured connection to a single fixed destination. This is a rigid restriction, and eventually a router is still needed at the destination to perform per-packet based switching/routing. The second disadvantage is the connection bandwidth utilization efficiency. Typically the circuit-based connection is setup and configured with a fixed bandwidth and cannot be dynamically changed based of the actual traffic usage. On the other hand, the packet traffic is typically very bursty. The pre-configured circuit to carry the packet is usually setup to carry the worst case traffic, which is the maximum bandwidth in the traffic pattern. In average, however, the real data traffic is typically much less than the worst case. The average bandwidth used is therefore only, e.g., 3/10 of the total connection bandwidth. In this way, using circuit connection to carry packet is very inefficient.

Packet Based Switching

Referring to Figure 1D, a prior art packet based switching design of using a centralized packet switching engine to do the switching for both the switching of circuit and packet. To support circuit switching, some circuit emulation through packet/cell is performed. A typical example is the ATM AAL1 circuit emulation used for circuit switching. More and more people are trying to use IP to emulate circuit for, e.g., voice over IP application.

Unify all traffic into a packet/cell based network is an ideal goal. It provides a simplified network infrastrcucture and all the mixed circuit/packet connection maintenance is saved. However, to support the quality of the voice connection using packets/cells a lot

of extra effort, and also need to enhance most of existing router/switch to eventually support it. This is still so far a difficult issue to resolve.

SUMMARY OF THE INVENTION

The present invention provides a dual switch architecture for mixed packet and circuit transports over SONET and SDH and DWDM. The dual switch architecture includes (1) a TDM circuit cross connect module, (2) a packet switch module, (3) interface modules with one or more ports, (4) a bi-directional TDM bus between the TDM circuit cross connect module and the packet switch module, (5) a point-to-point, bi-directional TDM connection between each interface module and the TDM circuit switch module, and (6) a point-to-point, bi-directional packet connection between each interface module and the packet switch module.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates a prior art hub structure.

Figure 1B illustratres a prior art switch structure.

Figure 1C illustrates a prior art circuit based switching design.

Figure 1D illustrates a prior art packet based switching design.

Figure 2 illustrates a dual-switch architecture in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Introduction

The invention described in co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-014 provides a system and method of virtually concatenating VT1.5s and STS-1s over SONET and SDH and WDM. The virtual concatenation invention allows users to setup connections or pipes with configurable bandwidth over either nxSTS-1/nxAU-3/nxAU-4 or nxVT1.5/nxTU-11/nxTU-12 within a nxSTS-1/nxAU-3/nxAU-4 pipe on an existing SONET/SDH network. This provides a connection or pipe of adjustable bandwidth with a granularity of close to 1.5 Mbps to fit the needs of applications. The resulting connection can be treated as a TDM like connection.

By replacing "STS-1" with "AU-3" or "AU-4" and "VT" or "VT1.5" with "TU-11" or "TU-12", the virtual concatenation invention applies to nxAU-3/nxAU-4 and nxTU-

11/nxTU-12 for SDH networks. For simplicity, these connections are called "nxVT" for both SONET and SDH networks. By replacing "STS-1" with "VT" or "VT1.5", the virtual concatenation invention applies to nxSTS-1 and nxAU-3/nxAU-4.

On top of the virtual concatenation invention, a dynamic bandwidth allocation (DBA) protocol, which is described in co-pending and commonly assigned U.S. Patent Application No. (Number to be assigned) with Attorney Docket Number 55369-015, allows for dynamically changing the throughput of all nxVT connections, based on the real-time traffic loads of applications using the nxVT connections. The DBA protocol allows for the efficient use of the SONET/SDH bandwidth through statistical multiplexing. The same dynamic bandwidth allocation protocol applies to nxSTS-1 and nxAU-3/nxAU-4.

The virtual concatenation invention provides for virtual concatenation, which includes creating a logical connection or pipe by combining multiple, n (where n is a positive integer), STS-1 or VT connections or pipes, which may be contiguous or non-contiguous, into a single connection or pipe, nxSTS-1 or nxVT, respectively, in order to support a connection or pipe with a higher throughput than the throughput of the original STS-1 or VT pipes.

Referring to Figure 2, the present invention provides a flexible dual-switch architecture used in a SONET access multiplexer to support mixed packet and circuit transport over SONET/DWDM ring. This architecture is used in Geyser Networks' SONET Access bandwidth Management (SABM) device to support aggregation of transport traffics from all kinds of interfaces, including T1, T3, Ethernet, OC-3, OC-12 and OC48. In this box, the traffic from each port on the interface card are treated as a mix of both pure TDM circuit and packet data connections. For TDM circuits, all data in the connection is treated as a byte stream. No packet format is interpreted to allow different processing on each packet. For packet connection, on the other hand, all packets are processed and forwarded separately. All null data samples between packets are discarded.

The present invention provides a dual packet/circuit switching architecture which allows simultaneous efficient switch of both circuit and packet connections. In this way, we avoid the disadvantage of circuit based or packet based switch for mix packet/circuit support and provide a practical feasible migration path to the future pure packet/cell based network. We leverage the existing SONET based network to support both circuit and packet connections, and on the other hand optimize the performance by allowing

dynamically assigning the bandwidth to either circuit or packet connection based on need. A more detailed description of the dual packet/circuit switching mechanism is described in the next section.

General

The dual packet/circuit switching architecture is defined to add/drop mixed circuit/packet traffic from/to local ports to/from SONET rings. In addition, some cross connect/switch/grooming functions are also performed such as:

- ☐ Mixed Circuit/Data Add/Drop Aggregation
- ☐ Circuit/packet cross-connect/switching
- ☐ Circuit/data connections flexibly/dynamically configurable as either TDM or DATA
- ☐ Circuit/data connections dynamically re-sizing
- ☐ Grooming in either circuit/data connection

The advantage of this design is as follows. First, the use of direct circuit mapping is used instead of circuit emulation like packet based switching. This provides all the circuit QoS needs without complex packet switch/router QoS support, therefore simplify the design. Secondly, unlike the circuit based switching that carry all the inflexibility for packet support, the dual packet/circuit switch perform the packet switching and flexibility switch the packets to any of the circuit connections. The circuit connection is dynamically set up/tear down/re-sized such that it truly reflects the actual traffic need. In this way the performance of packet switch is optimized. It has been studied that the performance of a mixed Circuit/Packet network is better than a pure packet/circuit network. The study, however, assumes separates circuit network and packet network. The proposal here is to use the same infrastructure to support mixed of circuit/packet connections, and perform dynamical re-configuration based on the traffic.

Dual Packet/Circuit Switch Architecture

In Figure 2, every port can be either packet or circuit interface. Every interface card has connections directly to both cross connect block and the packet switch block simultaneously. In case of circuit connections, the data is fed to the cross connection block directly through the red line. The cross connect card perform circuit cross connect and route the circuit to the trunk card for SONET ring. The trunk card is itself one of the

interface cards. In case of packet connection, the packet is buffered at the interface card and sent to the packet switch block through the blue line. The packet switch then perform all the packet switching to route each packet to its destination. Depending on where the destination, a packet can be switched back to an interface card through the blue line, or it can be switched to a circuit connection (red line between the switch block and the cross connect block). Once a packet is sent to the cross connect block, it is treated as a circuit connection, and switched by the cross connect to any line card and get onto the ring.

To summarize, the uniqueness of this architecture is as follows:

□ This architecture provides a platform to support both circuit and packet connection in parallel.

□ All circuit connections are switched like traditional TDM circuit.

□ All packets are terminated and packet switched. Depending on the destination/QoS, the circuit is fed into certain circuit. The circuit is then fed into the cross connect and forwarded to trunk card to go to the ring.

□ The total ring/port bandwidth is shared by both packet and circuit connections.

Depending on the implementation, the boundary between packet connection and circuit connection in a ring can actually be dynamically changed. This provides flexible allocation of bandwidth to either packet or circuit connections on the ring. The next section will describe more about the dynamical change of bandwidth allocation for either circuit or packet connection.

Another issue is about how a packet is mapped to a circuit through the cross connect after it goes through the packet switch engine. An example will be presented later to map our dual switch architecture to support mix of circuit connection and MPLS packet switching/routing.

Dynamical Circuit/Packet Bandwidth Allocation

One major advantage of mixed packet/circuit switching shows up when the bandwidth of either packet or circuit connection are dynamically configured based on demand. Whenever more circuit connections are needed, the packet switch connections can automatically reduce bandwidth usage to allocate more bandwidth for the circuit connections. The result is that more packets are sharing smaller data pipe, and increase a little bit delay in the data pipe. When less of circuit connections are needed, the unused bandwidth can be assigned to packet connections to allow more packet traffic to use the

bandwidth as best effort. This avoids the waste of unused bandwidth and allows over-subscription.

The virtual concatenation of VT1.5 and STS-1 and the dynamic bandwidth allocation (DBA) protocol provide good support to dynamically configure circuit/packet connections, and re-size the connections based on the real traffic on this dual switch architecture.

Dual Switch Architecture to support Mixed MPLS Switching and Circuit Connection

Combining the dual switch architecture with the dynamic bandwidth allocation, MPLS-based switching/routing architecture can be well supported. Basically all MPLS packets are switched/routed by the packet switch engine to forward packets according to the label. A logical circuit connection is setup up as a label switch path (LSP) on the ring to carry a forward equivalent class (FEC) of MPLS packets. In this way, all packets from the interface ports on a node element (NE) can be all aggregated into the same LSP as long as they share the same destination and the class of service (CoS). In this way, a fully meshed MPLS LSP network can be setup on the SONET ring through all the virtual concatenated logical connections.

In addition, the MPLS label distribution protocol (LDP) with bandwidth reservation capability can be used to dynamically increase/decrease/setup/tear down the virtual concatenated LSP according to the actual traffic need. This traffic need is processed by the Geyser device, taking into account the total bandwidth available based on the current use of both packet and circuit connections, a dynamic adjustment on the LSP bandwidth/quality can be made. With this, the Geyser's box can very flexibly be used to adjust the bandwidth allocation efficiently. For more details about the MPLS support, please refer to co-pending and commonly owned U.S. Patent Application No. (Number to be assigned), with Attorney Docket Number 55369-019, filed on August 16, 2001.

Summary

In summary, a dual-switching architecture is proposed here to flexibly support the mix of circuit connection and packet connections. This architecture is more flexible compared with the pure circuit based switching system. It is also much more simpler in supporting voice/video/TDM connections by avoiding the circuit emulation typically used in a pure packet based environment. By using the existing SONET hierarchy, it also

provides a very good migration path for carrier to carry mixed circuit/packet connection in the existing network.

By combining with other inventions such as dynamic bandwidth allocation and the MPLS mapping, the dual switch architecture will provide a very flexible and powerful platform in the next generation SONET network.

Conclusion

The present invention relates to optical networking. More particularly, the invention relates to a dual switch architecture for mixed packet and circuit transports over SONET and SDH and DWDM.

Having fully described a preferred embodiment of the invention and various alternatives, those skilled in the art will recognize, given the teachings herein, that numerous alternatives and equivalents exist which do not depart from the invention. It is therefore intended that the invention not be limited by the foregoing description, but only by the appended claims.

CLAIMS

We claim:

1. A dual switch architecture for mixed packeto and circuit transports over SONET and SDH and DWDM comprising:

a TDM circuit cross connect module;

a packet switch module;

interface modules with one or more ports;

a bi-directional TDM bus between the TDM circuit cross connect module and the packet switch module;

a point-to-point, bi-directional TDM connection between each interface module and the TDM circuit switch module; and

a point-to-point, bi-directional packet connection between each interface module and the packet switch module.

2. The dual switch architecture of claim 1 wherein the packet switch module comprises:

a packet mapping module which maps packets to TDM data; and

a packet demapping module which demaps TDM data to packets.

3. The dual switch architecture of claim 1 wherein the interface module can support TDM data and packets.

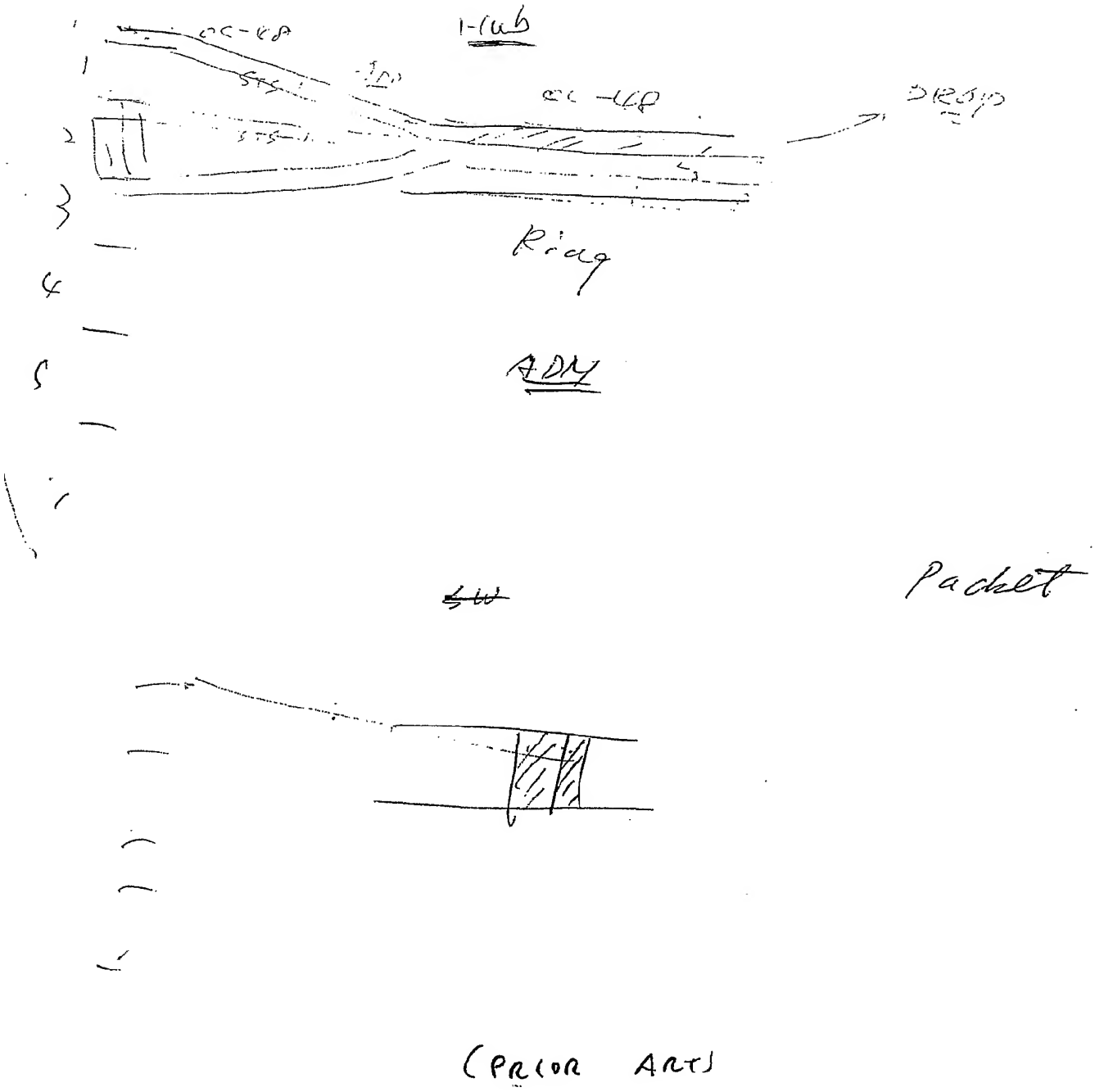
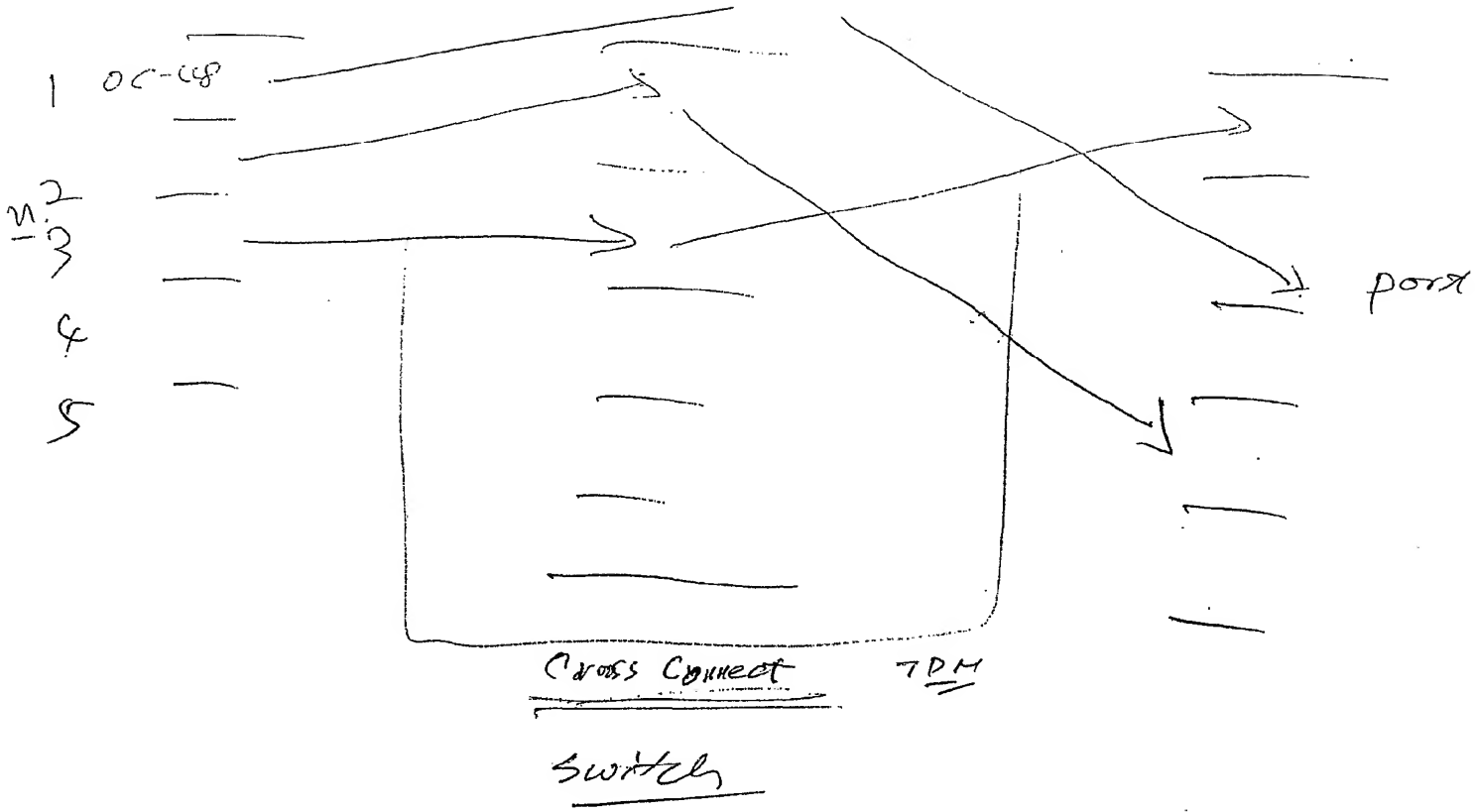
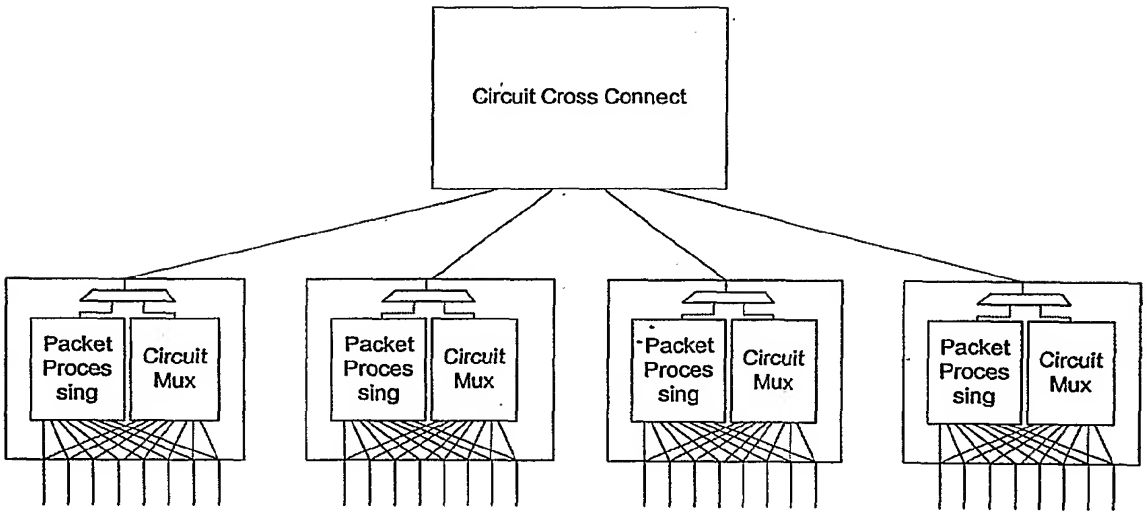


FIG. 1A



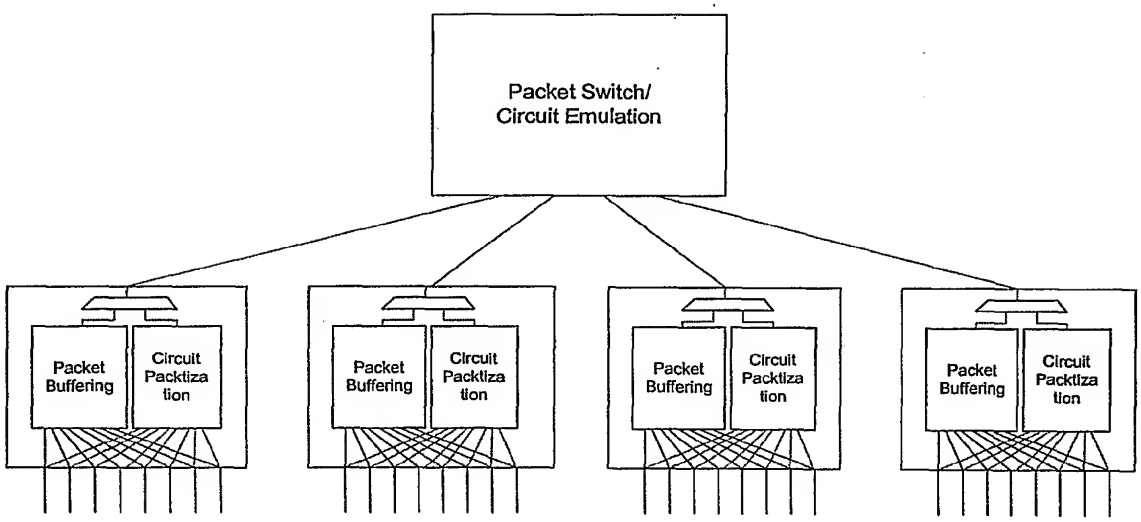
(PRIOR ART)

FIG. 1B



(PRIOR ART)

FIG. 1C



(PRIOR ART)

FIG.1D

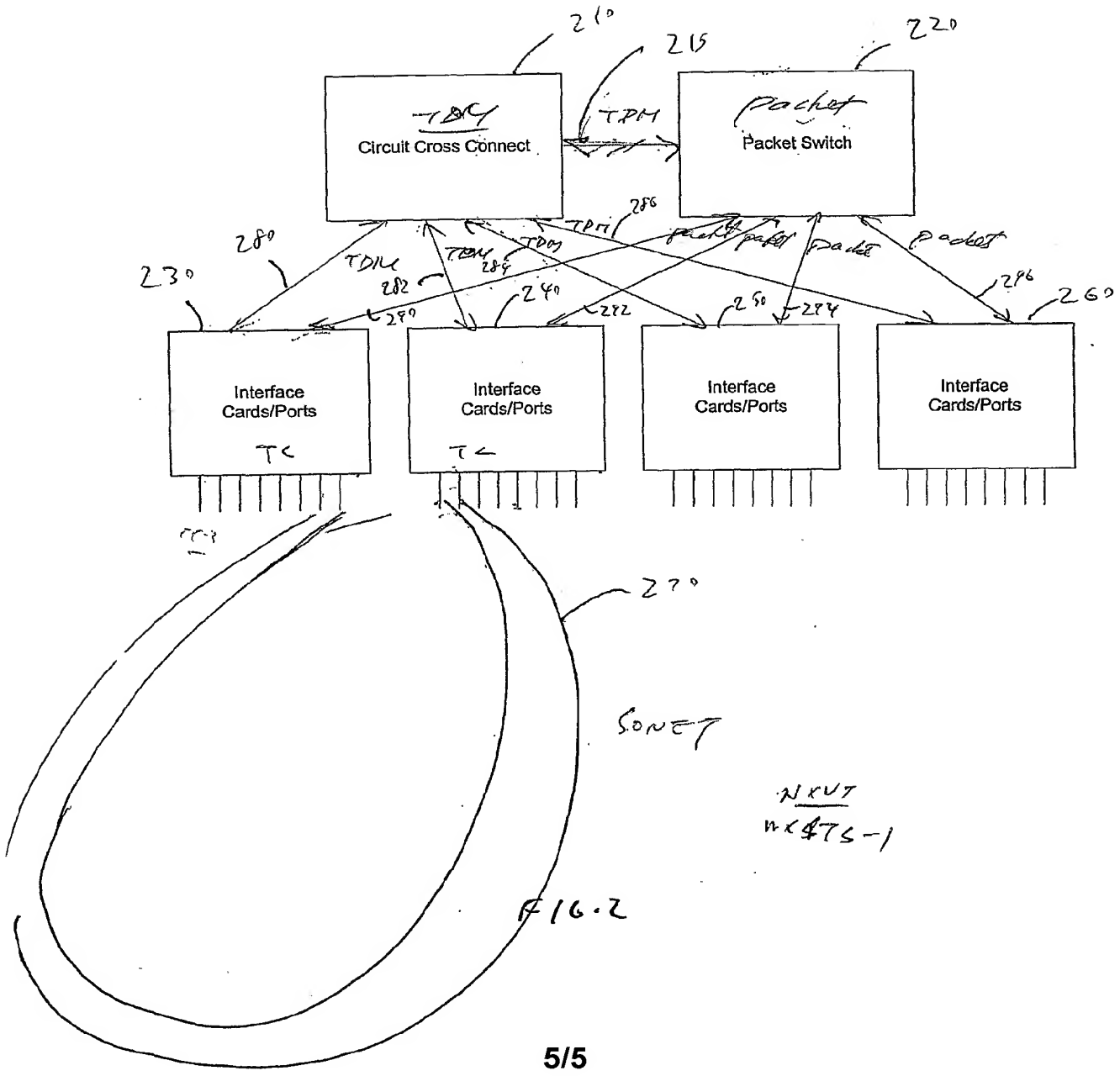

200
210
215
220
TDM
Circuit Cross Connect
TDM
Packet
Packet Switch
280
230
240
250
260
Interface Cards/Ports
Interface Cards/Ports
Interface Cards/Ports
Interface Cards/Ports
270
SONET
NxVT
nxDS-1

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/26567

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04L 12/64
US CL :370/352

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/352, 353, 354

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IEEE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST
search terms: dual switch, SONET, SDH, DWDM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,315,594 A (NOSER) 24 May 1994, col. 5, line 60-col. 7, line 4.	1-3
A	US 4,731,785 A (FERENC et al) 15 March 15, 1998, col. 4, line 18-col. 6, line 36.	1-3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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Date of the actual completion of the international search 15 NOVEMBER 2001	Date of mailing of the international search report 06 DEC 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SOON-DONG HYUN Telephone No. (703) 308-0000

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